100Gb/s QSFP28 SR4 850nm 100m

PRODUCT FEATURES

- 4 independent full-duplex channels
- Up to 28Gb/s data rate per channel
- QSFP28 MSA compliant
- Compliant to IEEE 802.3bm 100GBASE-SR4
- Up to 100m OM4 MMF transmission
- Operating case temperature: 0 to 70oC
- Single 3.3V power supply
- Maximum power consumption 3.5W
- MTP/MPO optical connector
- RoHS-6 compliant

APPLICATIONS

- Rack to Rack
- Data Center
- Infiniband QDR, DDR and SDR
- 100G Ethernet

GENERAL DESCRIPTION

This product is a parallel 100Gb/s Quad Small Form-factor Pluggable (QSFP28) optical module. It provides increased port density and total system cost savings. The QSFP28 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 25Gb/s operation for an aggregate data rate of 100Gb/s on 100 meters of OM4 multi-mode fiber.

An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP28 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an MSA compliant 38-pin edge type connector.

The module operates by a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

FUNCTION DESCRIPTION

This product converts parallel electrical input signals into parallel optical signals, by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also

voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 25Gb/s per channel. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP28 module must be used.
Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

ORDERING INFORMATION

Product Part Number	Data Rate	Media	Wavelength	Transmission Distance	Temperature Range（Tcase）
ZQSP851T-MDS1	103.1G	MMF	850	100m	0~70℃

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d	3.4		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

RECOMMENDED OPERATING CONDITIONS AND POWER SUPPLY REQUIREMENTS

Parameter	Symbol	Min	Typical	Max	Units
Operating Case Temperature	T_{OP}	0		70	degC
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate, each Lane			25.78125	28.05	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance (OM3 MMF)	D1			70	m
Link Distance (OM4 MMF)	D2			100	m

ELECTRICAL INPUT/OUTPUT CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
Power Consumption				3.5	W	
Supply Current	Icc			1060	mA	
Transceiver Power-on Initialization Time				2000	ms	1
Transmitter (each Lane)						
Single Ended Input Voltage Tolerance (Note 2)		-0.3		3.6	V	
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	180		1000	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Total Jitter				0.40	UI	
Deterministic Jitter				0.15	UI	
Receiver (each Lane)						
Single Ended Output Voltage		-0.3		4	V	
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		900	mVpp	

Differential Output Impedance	Zout	90	100	110	Ohm	
Total Jitter				0.3	UI	
Deterministic Jitter				0.15	UI	

Note 1) Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
Note 2) The single ended input voltage tolerance is the allowable range of the instantaneous input signals

OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Transmitter						
Center Wavelength	λ_C	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda_{rms}$			0.6	nm	
Average Launch Power, each Lane	P_{AVG}	-8.4		2.4	dBm	
Optical Modulation Amplitude (OMA), each Lane	P_{OMA}	-6.4		3.0	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			4.0	dB	
Launch Power in OMA minus TDEC, each Lane		-7.3			dBm	
Transmitter and Dispersion Eye Closure (TDEC), each Lane				4.3	dB	
Extinction Ratio	ER	2.0			dB	
Optical Return Loss Tolerance	TOL			12	dB	
Encircled Flux		≥ 86% at 19um ≤ 30% at 4.5um				
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}, 5×10^{-5} hits/sample		{0.3,0.38,0.45,0.35,0.41,0.5}				2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Center Wavelength	λ_C	840	850	860	nm	
Damage Threshold, each Lane	TH_d	3.4			dBm	3

Average Receive Power, each Lane		-10.3		2.4	dBm	
Receiver Reflectance	R_R			-12	dB	
Receive Power (OMA), each Lane				3.0	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-5.2	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-13	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 5):						
Stressed Eye Closure (SEC), Lane under Test			4.3		dB	
Stressed Eye J2 Jitter, Lane under Test			0.39		UI	
Stressed Eye J4 Jitter, Lane under Test				0.53	UI	
OMA of each Aggressor Lane			3		dBm	
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.28,0.5,0.5,0.33,0.33,0.4}				

Note 1) Even if the TDP < 0.9 dB, the OMA min must exceed the minimum value specified here.
Note 2) See Figure 5 below.
Note 3) The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
Note 4) Measured with conformance test signal at receiver input for BER = 1x10-12.
Note 5) Stressed eye closure and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

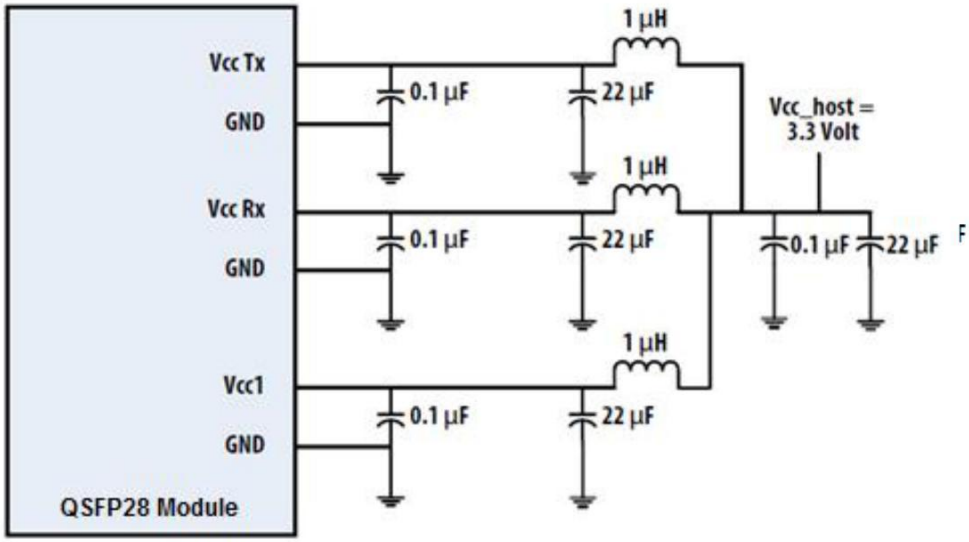
DIGITAL DIAGNOSTIC FUNCTIONS

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

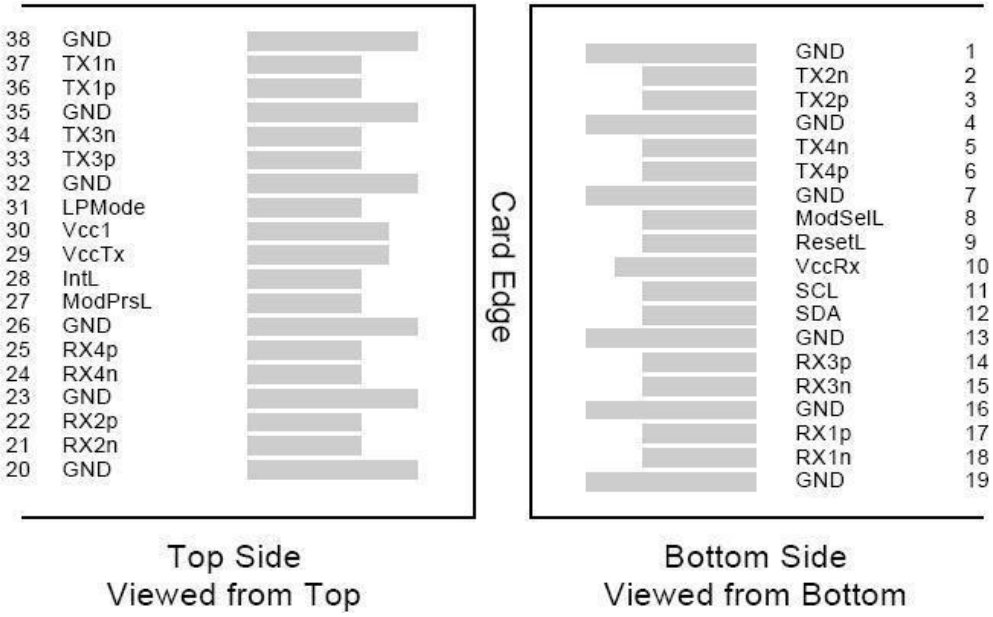
Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.15	0.15	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	Ch1~Ch4
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Note 1) Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

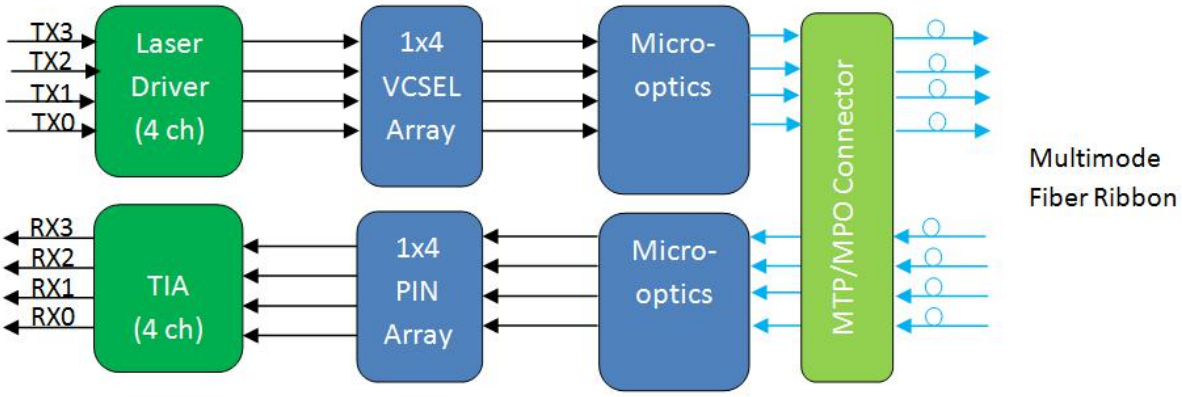
RECOMMENDED POWER SUPPLY FILTER



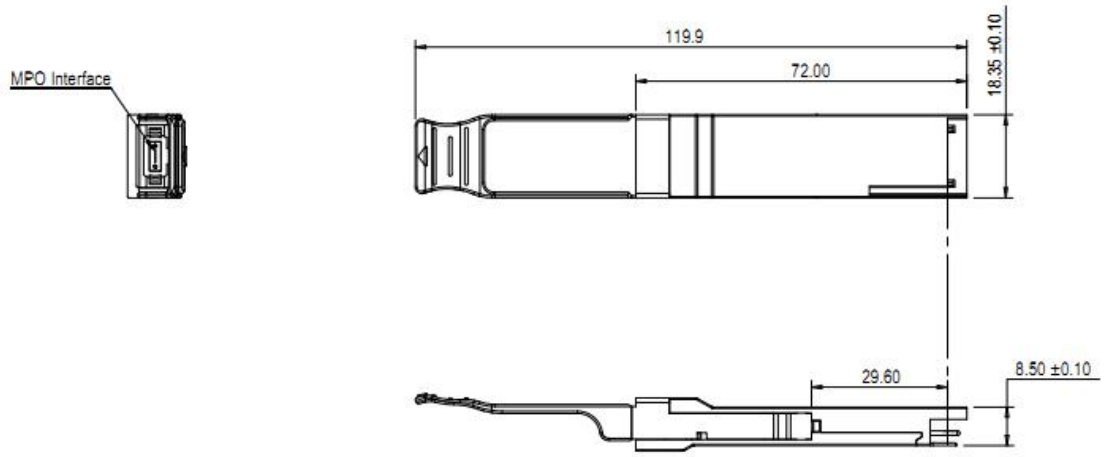
PIN DEFINITIONS AND FUNCTIONS



TRANSCEIVER BLOCK DIAGRAM



MECHANICAL DIMENSIONS



Optical Interface Lanes and Assignment

Figure 1 shows the orientation of the multi-mode fiber facets of the optical connector. Table 1 provides the lane assignment.

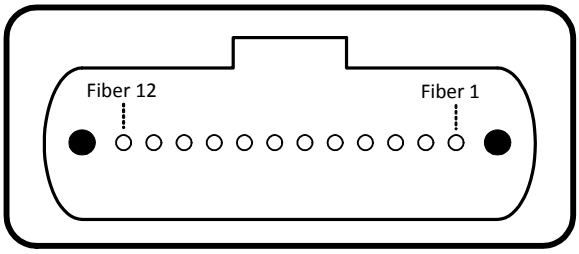


Figure 1. Outside View of the QSFP28 Module MPO Receptacle

Table 1: Lane Assignment

Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5,6,7,8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

FOR MORE INFORMATION

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